REMARKS

Applicants have studied the Office Action dated August 25, 2004, and have made amendments to the claims. Claims 1-7 and 9-16 are pending. Claims 1, 8, 9 and 16 are independent claims. Claims 1-7 and 9-16 have been amended. Claims 8 and 17 have been canceled without prejudice. No new matter has been entered. It is submitted that the application, as amended, is in condition for allowance. Reconsideration and reexamination are respectfully requested.

Amendments to Drawings

Amendments were made to the FIGS. 1 and 2 in response to objections by the Examiner. Amendments were made to FIG. 5 to provide clarification of the invention and better correspondence between the steps of the illustrated method and the disclosure in the specification as originally filed. No new matter has been added as the amendments have support in the application as originally filed.

Amendments to Specification

Amendments have been made to the specification and two copies of a substitute specification have been provided. One copy of the substitute specification indicates change markings where amendments were made and one copy is a clean copy of the specification as amended. The amendments were made in response to objections by the Examiner and to correct grammatical and typographical errors and provide a more concise description of the invention. No new matter as been added as the amendments have support in the application as originally filed.

Objection to Drawings

The Examiner objected to in the drawings as being mislabeled and as failing to comply with 37 CFR § 1.84(p)(5) as not including references mentioned in the description. Specifically, the Examiner asserted that FIG. 1 is mislabeled as "BACKBOUND ART" and suggested that "BACKBOUND" be changed to "BACKGROUND." Furthermore, the Examiner asserted that the "break point address" and "break point enable signal" outputted to the memory break controller disclosed at page 8, line 17 of the specification are not included in the drawings.

With this paper, FIG 1 has been amended to replace "Backbound" with "Related." Furthermore, FIG. 2 has been amended to indicate that the "CONTROL" and "BREAK" signals are bi-directional, thereby illustrating the "break point address" and "break point enable signal" outputted to the "MEMORY BREAK CONTROLLER" from the "DEBUGGER CONTROLLER." It is respectfully submitted that the grounds for objection have been overcome and it is respectfully requested that the Examiner withdraw the objections.

Objection to Specification

The Examiner objected to the specification as failing to comply with 35 U.S.C. § 112, first paragraph, in that it contains terms that are not clear, concise and exact. Specifically, the Examiner asserted that unclear, inexact and verbose terms are used, for example:

The phrase "observing a change of state and flow of an address and a data of the specific data memory in a data memory" at page 3, ll. 22-23.

The phrase "host computer 10 is being operation" at page 8, ll. 9-10.

The phrase "According to judgment result, in case that the processor core 40 writes a data" at page 9, ll. 19-20.

The phrase "The data of a specific address of the data memory (70) read by the processor core 40 has an arithmetic and logical operation relation with a data value of a difference address or a correlation with a specific address of the data memory 70" at page 10, ll. 4-7.

The phrase "In case of executing continuously, the memory break controller 50 reads A2, so that addresses of every memory related until the next A2 value is written and their contents are outputted" at page 12, ll. 17-19.

The phrase "an error that an erroneous calculation is inputted a during processing or a data memory is erroneously assigned is quickly sensed" at page 14, ll. 7-8.

The phrase "a program development environment is set similar to an environment that the processor is substantially operated. Thus, a time and an expense for developing a program can be also saved" at page 14, ll. 11-13.

With this paper, the specification has been amended to clarify the phrases indicated by the Examiner and to use more exact language in order to clearly disclose the invention. Furthermore, as indicated in the substitute specification submitted with this response, the specification has been amended throughout in order to more clearly disclose the invention using exact language.

The Examiner further asserted that the example program beginning on the bottom of page 11 is unclear and appears illogical in places. The Examiner asserted the following sources of confusion:

The equation A2 = A2 + (A1*A2) appears illogical and requires more explanation.

The language "the memory break controller 50 reads A2, so that addresses of every memory related until the next A2 value is written and their contents are outputted" on page 12, ll. 17-19 is difficult to interpret.

A2 is at times treated as a value, such as at page 13, line 2, and at times treated as a system component capable of performing functions, such as at page 13, ll. 7-8.

With this paper, the description of the program on pages 11-13 has been amended to clearly indicate that A2 represents a memory location in which a value is stored. Furthermore, an overview of the four steps that comprise the program has been added at page 12, line 4 in order to more clearly disclose how the formula is implemented. The overview is an interpretation of the four steps as disclosed in the application as originally filed in view of FIG. 5 as originally filed and no new matter has been added. Moreover, the specification has been amended to more clearly disclose of the debugging of the program on page 12, line 5, to page 13, line 16 as supported by the disclosure in the application as filed, specifically FIG. 5.

No new matter has been added as the amendments merely delete unnecessary text, replace some text words and phrases with similar text and phrases, and re-arrange the existing text in order to make the meaning less ambiguous. It is respectfully submitted that the grounds for objection have been overcome and it is respectfully requested that the Examiner withdraw the objections.

Claim Objections

The examiner objected to the claims due to informalities. Specifically, the Examiner asserted the following:

The word "data" is a plural noun and should not be referred to as "a data" as was done in line 1 of claim 1, line 2 of claim 3, line 6 of claim 8, lines 6 and 7 of claim 11, lines 5-7 of claim 12, line 1 of claim 13, line 1 of claim 14, line 1 of claim 15, lines 11-13 of clam 16, and line 1 of claim 17. The Examiner suggested changing the phrase "a data" to either "the data" or "data."

With this paper, claims 1, 3, 8, and 11-17 have been amended as suggested by the Examiner. It is respectfully submitted that the grounds for objection have been overcome and it is respectfully requested that the Examiner withdraw the objections.

Claims 2, 5, 6 and 10 were objected to as dependent on base claims to which the Examiner has objected.

It is respectfully submitted that the grounds for objection to the base claims have been overcome and it is respectfully requested that the Examiner withdraw the objection.

§ 112, First Paragraph Rejections

The Examiner rejected claims 7, 11-14 and 17 under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification in a way as to enable one skilled in the art to which the claims pertain, or with which they are most nearly connected, to make and/or use the invention. Specifically, the Examiner made the following assertions:

Claim 7 recites "it outputs addresses and data of every memory which are read from or written in the processor core," which suggests multiple memories, while the specification specifically states that the debugging apparatus includes a single data memory. The Examiner suggested amending the limitation to read "it outputs every address and data which is read from or written to the data memory by the processor core."

With this paper, claim 7 has been amended to recite "the addresses and corresponding data of every memory location accessed by the processor is output," thereby referring to multiple address locations in a single data memory. It is respectfully submitted that claim 7 is now in compliance with the first paragraph of § 112.

Claim 11 recites that two addresses are compared, found to be identical, and are then compared again after possibly setting flags, with the claim indicating that the two addresses may no longer be identical even though no explanation is provided in the claim language or specification for why the addresses may no longer be identical.

With this paper, claim 11 has been amended to further recite that the processor is re-activated and a subsequently accessed memory address is compared to the first address such that claim 11 more clearly discloses the method of the present invention as disclosed in the application as originally filed. It is respectfully submitted that claim 11 is now in compliance with the first paragraph of § 112.

The phrase "next data memory" in claims 13 and 17 suggests multiple memories, which is contrary to the disclosure in the specification. The Examiner suggested amending the claims to recite "a next data address of the data memory to be used."

With this paper, claim 13 as been amended to recite "the next data memory location accessed," thereby referring to multiple address locations in a single data memory. It is

respectfully submitted that claim 13 is now in compliance with the first paragraph of § 112. Furthermore, claim 17 has been canceled without prejudice with this paper, thereby rendering the rejection moot with respect to the claim.

Claims 12-14 are dependent on a rejected claim.

It is respectfully submitted that the grounds for objection to base claim 11 have been overcome and it is respectfully requested that the Examiner withdraw the objection.

§ 112, Second Paragraph Rejections

The Examiner rejected claims 1-17 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly clam the subject matter which the applicant regards as the invention. Specifically, the Examiner made the following assertions:

The phrase "when the address is sensed to be identical" at lines 10-11 of claim 1 is confusing since it is unclear what the address is sensed to be identical to and, if the address is sensed to be identical to the break point address, the phrase is redundant given the limitation "recognizing an address as a break point address." The Examiner suggested deleting the phrase from the claim.

With this paper, claim 1 has been amended, as suggested by the Examiner, to delete the phrase. It is respectfully submitted that claim 1 is now in compliance with the second paragraph of § 112.

There is insufficient antecedent basis for the limitation "the control signal" in line 4 of claim 5. The Examiner suggested amending the claim to recite "a control signal."

With this paper, claim 5 has been amended, as suggested by the Examiner. It is respectfully submitted that claim 5 is now in compliance with the second paragraph of § 112.

There is insufficient antecedent basis for the limitation "the data of the break point address" in line 10 of claim 5 and line 14 of claim 8. The Examiner suggested amending the claims to either recite an additional limitation to describe data being sent with the break point address value or to recite "storing data that corresponds to the break point address."

With this paper, claim 5 has been amended to recite "data stored at the break point address." It is respectfully submitted that claim 5 is now in compliance with the second paragraph of § 112. Furthermore, claim 8 has been canceled without prejudice with this paper, thereby rendering the rejection moot with respect to the claim.

The phrase "when the address trace check flag is enabled, it outputs addresses and data of every memory" at lines 1-2 of claim 7 is indefinite as to what the word "it" refers. The

Examiner suggested replacing "it" with an appropriate identifier for the component of the apparatus that "outputs addresses and data."

With this paper, claim 7 has been amended to delete the word "it" such that the claim recites "when the address trace check flag is enabled, the addresses and corresponding data of every memory location accessed by the processor are output," thereby eliminating the word which the Examiner asserted was indefinite. It is respectfully submitted that claim 7 is now in compliance with the second paragraph of § 112.

The phrase "outputting an address of a data memory to be observed, that is a break point address and a break enable signal" at lines 2-3 of claim 9 is indefinite as to what the word "that" refers. The Examiner suggested amending the claim to recite "outputting a break enable signal and a break point address of a data memory to be observed, when a processor is switched to a debugging mode." Furthermore, there is insufficient antecedent basis for the term "processor core" in claim 9 as it is unclear whether the term "processor" at lines 3, 5 and 16 of the claim refers to the same entity as the "processor core" at lines 10, 12, 13 and 15. Moreover, the terms "processor" and "processor core" are used interchangeably throughout the dependent claims.

With this paper, claim 9 has been amended in a manner similar to that suggested by the Examiner and the term "processor core" has been changed to "processor" throughout the specification, claims and drawings. It is respectfully submitted that claim 9 is now in compliance with the second paragraph of § 112.

There is insufficient antecedent basis for the phrases "the address trace check flag," "the data check flag" and "the memory break control register" in lines 7-8 of claim 11. The Examiner suggested that claim 11 should be dependent on claim 10 instead of claim 9.

With this paper, claim 11 has been amended as suggested by the Examiner to depend from claim 10. It is respectfully submitted that claim 11 is now in compliance with the second paragraph of § 112.

There is insufficient antecedent basis for the phrase "the step of comparing address" at line 1 of claim 12 as it is unclear to which step in claim 11 the phrase refers.

With this paper, claim 12 has been amended to replace the phrase "wherein the step of comparing address comprises" with "further comprising," thereby eliminating the phrase that the Examiner asserted was unclear. It is respectfully submitted that claim 12 is now in compliance with the second paragraph of § 112.

The phrase "in case of reading a data upon judgment" at lines 1-2 of claims 13 and 17 creates confusion as to when the event of reading data takes place. The Examiner suggested amending the claims to recite "wherein, if the processor core reads the data."

With this paper, claim 13 has been amended in a manner similar to that suggested by the Examiner. It is respectfully submitted that claim 13 is now in compliance with the second paragraph of § 112. Furthermore, claim 17 has been canceled without prejudice with this paper, thereby rendering the rejection moot with respect to the claim.

The phrase "in case of writing a data in the judging step" at line 1 of claim 14 creates confusion as to when the event of writing data takes place. The Examiner suggested amending the claim to recite "wherein, if the processor core writes the data."

With this paper, claim 14 has been amended in a manner similar to that suggested by the Examiner. It is respectfully submitted that claim 14 is now in compliance with the second paragraph of § 112.

The phrase "a step in which a processor is switched into a debugging mode, an address of a data memory to be observed, that is, a break point address, and a break enable signal are outputted" at lines 3-5 of claim 16 is unclear as it is indefinite as to what is being outputted. The Examiner suggested amending the claim to recite "a step in which when a processor is switched into a debugging mode, a break point address of a data memory to be observed and a break enable signal are outputted."

With this paper, claim 16 has been amended to recite "switching a processor to a debugging mode and outputting a break point address of a data memory to be observed and a break enable signal." It is respectfully submitted that claim 16 is now in compliance with the second paragraph of § 112.

Claims 2-4, 6, 10 and 15 are dependent on a rejected base claim.

It is respectfully submitted that the grounds for objection of the base claims have been overcome and, therefore, claims 2-4, 6, 10 and 15 are now in compliance with the second paragraph of § 112.

§ 102 Rejections

Claims 1, 2, 5, 6, 8-12 and 14 were rejected under 35 U.S.C. § 102(e) as being anticipated by Waldie et al. (U.S. Patent Publication 2002/0065646 A1). This rejection is respectfully traversed.

It is respectfully noted that a proper rejection for anticipation under § 102 requires complete identity of invention. The claimed invention, including each element thereof as recited

in the claims, must be disclosed or embodied, either expressly or inherently, in a single reference. Scripps Clinic & Research Found. v. Genentech Inc., 927 F.2d 1565, 1576, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991); Standard Havens Prods., Inc. v. Gencor Indus., Inc., 953 F.2d 1360, 1369, 21 U.S.P.Q.2d 1321, 1328 (Fed. Cir. 1991).

With regard to claim 8, it is respectfully noted that the claim 8 has been canceled without prejudice with this paper and the rejection is, therefore, moot with respect to the claim.

With regard to independent claims 1 and 9, it is respectfully noted that with this paper, those claims have been amended to recite that the address and corresponding data of each data memory location accessed by the processor is output until another break point address is reached. Support for the amendments is found in the application as originally filed in claims 7 and 15. It is respectfully submitted that Waldie et al. fails to disclose this limitation.

It is respectfully noted that in the Office action, at pages 24 and 26, the Examiner states, with respect to the § 103 rejections of claims 7 and 15, that Waldie et al. fails to explicitly teach this limitation and asserts that Waldie et al. teaches, at paragraph 75, that the host computer may examine the results in the debug system storage registers in the background during a debugging event. It is respectfully submitted that the teachings of Waldie et al. regarding the host computer "examining" the results in the storage resisters is not the same as outputting the address and corresponding data of each data memory location accessed by the processor until another break point addressed is reached, as recited in independent claims 1 and 9.

It is respectfully noted that Waldie et al. discloses, at paragraph 75, only that the state of the processor system may be inspected "[w]hen an event trigger is generated." It is respectfully submitted that nowhere in Waldie et al. is if taught or disclosed that the state of the processor system may be output to the host computer **while** the processor is operating, a patentably different process that is required by the limitation recited in independent claims 1 and 9 of the present invention.

Therefore, it is respectfully asserted that independent claims 1 and 9 are allowable over the cited reference. It is further respectfully asserted that claims 2, 5 and 6, which depend from claim 1, and claims 10-12 and 14, which depend from claim 9, also are allowable over the cited reference.

§ 103 Rejections

Claims 3, 4, 7, 13 and 15-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Waldie et al. in view of Torrey et al. (U.S. Patent No. 6,145,123). This rejection is respectfully traversed.

With regard to claim 17, it is respectfully noted that the claim 17 has been canceled without prejudice with this paper and the rejection is, therefore, moot with respect to the claim.

With regard to independent claim 16, it is respectfully noted that with this paper, the claim has been amended to recite outputting the address and corresponding data of each data memory location accessed by the processor until another break point address is reached. Support for the amendment is found in the application as originally filed in claims 7 and 15. It is respectfully submitted that neither Waldie et al. nor Torrey et al. disclose this limitation.

It is respectfully noted that the Examiner, at page 31, states that Waldie et al. fails to explicitly teach this limitation and asserts that Waldie et al. teaches, at paragraph 75, that the host computer may examine the results in the debug system storage registers in the background during a debugging event. As previously asserted with regard to independent claims 1 and 9, the teachings of Waldie et al. regarding the host computer "examining" the results in the storage resisters is not the same as outputting the address and corresponding data of each data memory location accessed by the processor until another break point address is reached, as recited in independent claim 16.

It is further respectfully noted that the Examiner, at pages 22, 24, 26 and 31 of the Office action, asserts, with respect to the §103 rejection of, respectively, claims 3, 7, 15 and 16, that Torrey et al. teaches "trace information" that is analogous to the address and data of the data memory. The Examiner's interpretation of Torrey et al. is respectfully traversed.

It is respectfully submitted that the trace information captured by the trace unit 140 of Torrey et al. is not address and data information related to data memory, but rather program instructions in program memory executed by the processor. It is further respectfully submitted that the present invention, by enabling the actual data memory addresses and data to be monitored and output to the host computer, is an improvement over conventional systems such as Torrey et al., which are not capable of recognizing the data flow to data memory. See specification at page 3, ll. 8-15.

Therefore, it is respectfully asserted that Torrey et al. fails to cure the deficiencies of Waldie et al. with respect to outputting the address and corresponding data of each data memory location accessed by the processor until another break point address is reached, as recited in independent claims 1, 9 and 16 and dependent claims 3, 7 and 15. It is further respectfully asserted that independent claim 16 is allowable over the cited references. Moreover, it is respectfully asserted that claims 3, 4 and 7, which depend from claim 1, and claims 13 and 15, which depend from claim 9, also are allowable over the cited references.

CONCLUSION

In light of the above remarks, Applicant submits that claims 1-7 and 9-16 of the present application are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

U.S. Patent Publication 2002/0188813 A1 (Cheung et al.) has been cited as having been made of record and not relied upon. Applicant respectfully submits that the Cheung et al. Publication, having been filed after the present application, would not be a valid reference. Furthermore, Applicant has reviewed the Cheung et al. publication and believes that the claims of the present invention are allowable over the Cheung et al. publication individually or in combination with the other cited references.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein; and no amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 623-2221 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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Encl: Substitute FIGS. 1, 2, 5

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IN THE DRAWINGS:

Substitute drawing sheets are enclosed for FIGS. 1, 2 and 5 to replace the original drawing sheets filed with the application. No new matter has been added.

Specifically, the following amendments have been made:

FIG. 1: The word "BACKBOUND" has been replaced with the word "RELATED" and the word "core" has been deleted from the description of the element referred to by reference numeral 4.

FIG. 2: The word "core" has been deleted from the description of the element referred to by reference numeral 40. Arrows between Debugger controller and Memory Break Controller were amended to illustrate the bi-directional data flow for the CONTROL and BREAK signals.

FIG 5: The description for steps S10-S14, S16 and S19 has been amended to provide further clarification of the invention.